

Appl. No. 10/721,876
Examiner: Lum, Leon Yun Bon, Art Unit 1641
In response to the Office Action dated July 14, 2006

Date: October 12, 2006
Attorney Docket No. 10116401

further clarify and distinguish Applicant's invention over the prior art relied upon by the Examiner in the Final Office Action in hopes of avoiding an unnecessary appeal process for this case.

Reconsideration of this application is respectfully requested in light of the following remarks.

Rejections Under 35 U.S.C. 103(a)

Claims 25-26 and 28-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada in view of Snow. Claims 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada in view of Snow and in further view of Tsuruta. Applicant respectfully traverses the rejections for the reasons as follow.

MPEP 2142 reads in part:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In connection with the third criteria, MPEP 2143.03 goes on the state:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Claim 25 recites, *inter alia*, a ceiling gate dielectric layer comprising a first ceiling gate dielectric layer and a second ceiling gate dielectric layer portion positioned on the drain and the source, respectively; and a ceiling gate positioned on the ceiling gate dielectric layer.

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In the rejections, the Examiner identifies electrode 50 of Snow as the alleged the ceiling gate of claim 25. This position was traversed in the last paragraph on page 10 of the amendment filed on April 20, 2006, wherein Applicant argued that Snow does not teach the claimed ceiling gate of claim 25 since Snow expressly teaches a gateless FET.

In Final Office Action, the Examiner states that electrode 50 meets Snow's definition of a gate and that Snow teaches a gateless FET only in the context that there is no gate above the active channel. As Applicant understands the office action, it is the Examiner's position that Snow teaches that the definition of a "gate" is a "conductive layer," and that therefore any conductive layer is a gate.

In response, Applicant respectfully submits that the Examiner is mischaracterizing both the definition of a gate in the relevant art and Snow's teaching.

Applicant first submits that, by definition, a "gate" controls the flow of electrical current between a source and drain by gate bias. Thus, in order to function as a gate, an electrode cannot be directly connected to the source/drain.

However, as shown in Fig. 1 and described in col. 3, lines 63-64 of Snow:

... Electrodes 50 connect to the source 12, drain 14, and body contact 40 ...

As electrodes 50 in Snow connect to the source/drain directly, and therefore do not provide gate bias or function to control the electrical current between the source and drain, Applicant submits that electrodes 50 cannot be interpreted as a "gate" as recited in claim 25. To the contrary, electrodes 50 merely serve as source electrodes, drain electrodes, and contact electrodes.

Secondly, Applicant submits that Snow does not in fact define a gate as merely "a conductive layer". Rather, in col. 3, lines 23-25, Snow describes that a conventional FET has a conductive layer serving as a gate. To the contrary, in the gateless FET of Snow, the gate bias is not provided by a gate electrode (i.e., a conductive layer), but instead by the sample solution. In this regard, see col. 4, lines 7-10 of Snow, which read:

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... The sample solution itself provides the gate bias, and it is not required that a threshold voltage be overcome in order to supply source-to-drain current ...

Thus, the sentence "[no] such gate is present in the present invention" in col. 3, lines 26-27 of Snow clearly refers to the absence of a conductive layer serving as a gate in the FET, rather the absence of a conductive layer serving as a gate in a certain location of the FET (i.e., above the active channel), as argued by the Examiner.

In short, Snow expressly teaches a FET in which there is no gate electrode (i.e., no conductive layer providing gate bias). If there is no gate taught in Snow, Applicant submits that Snow cannot be relied upon to teach the ceiling gate as recited in claim 25.

It is therefore Applicant's belief that even when taken in combination, the prior art references relied upon by the Examiner do not teach or suggest all the limitations of claim 25. For at least this reason, a *prima facie* case of obviousness cannot be established in connection with this claim. Furthermore, as it is Applicant's belief that a *prima facie* case of obviousness is not established for claim 25, the Examiner's arguments in regard to the dependent claims are considered moot and are not addressed here. Allowance of claims 25-35 is respectfully requested.

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Conclusion

For the reasons described above, the Applicant believes that the application is now in condition for allowance and respectfully requests so.

Respectfully submitted,



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